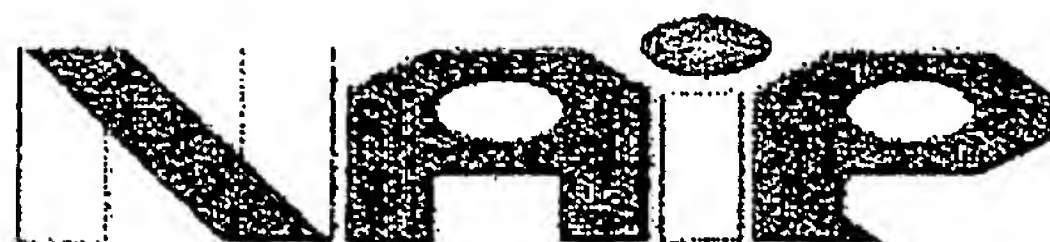


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**North America
Intellectual Property Corporation**

.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

FAX: 806-498-6673

e-mail: winstonhsu@naipo.com

Customer No.: 27765

Fax To: MIS, DAVID C

Tel.: (571) 272-1765

Art Unit: 2817

Fax: (571) 273-8300

From : Winston Hsu, Registration No. 41,526

Serial No.: 10/710,934

Patent No.: 7,075,375

Attorney Docket No.: MTKP0173USA

Subject: Citation of Prior Art under 37 CFR §1.501.

Total Pages: 32 pages (including cover page)

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PTO/SB/21 (09-04)

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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Patent Number	7,075,375	
	Issue Date	07/11/2006	
	First Named Inventor	Hong-Ching Chen	
	Art Unit	2817	
	Examiner Name	MIS. DAVID C	
Total Number of Pages in This Submission	3	Attorney Docket Number	MTKP0173USA

ENCLOSURES (Check all that apply)		
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Hong-Ching Chen, et al.

5 Patentee: MEDIATEK INCORPORATION

Patent No.: 7,075,375

Issue Date: 07/11/2006

Appl. No.: 10/710,934

Filing Date: 08/13/2004

Docket No.: MTKP0173USA

Confirmation No.: 4933

10 Title: PHASE LOCKED LOOP FOR CONTROLLING AN OPTICAL
RECORDING DEVICE AND METHOD THEREOF

To: Commissioner for Patents

P.O. BOX 1450

Alexandria, VA 22313-1450

15

Subject: Submission of Prior Art under 37 CFR §1.501

Dear Sir,

20

The undersigned agent hereby submits the prior arts
as cited in the Office Action issued on 10/13/2006
against the counterpart CHINA patent application no.
2005100535318. A form PTO/SB/42 detailing prior arts
25 cited, copies of the patents or printed publications,
and any necessary English translation are attached

pursuant to 37 CFR 1.501 and MPEP 2205.

It's believed that the prior arts cited in the Office Action are pertinent and applicable to the patentability of the claims of the above-identified patent. It is the patentee's desire to have the citation of prior art placed in the patent file.

10 Respectfully submitted,



Date: DEC. 13 2006

Winston Hsu, Patent Agent No. 41,526

15 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

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HASE LOCKED LOOP for CONTROLLING RECORDABLE OPTICAL DISK
DRIVE

A phase locked loop (PLL) for generating an oscillation signal such that the oscillation signal maintains a substantially constant phase difference with respect to a phase of a reference signal. The PLL includes a first frequency divider for dividing a frequency of the oscillation signal by a first divisor, and for generating a number of multiphase signals, such that each multiphase signal is out of phase with each of the other multiphase signals, a phase shift detection circuit for comparing a phase of the oscillation signal with the phase of the reference signal, and a phase adjusting circuit for selecting one of the multiphase signals generated by the first frequency divider to be an output signal such that the PLL is able to reduce the phase difference between the oscillation signal and the reference signal.